

**IN THE CLAIMS:**

1. (Currently amended) A method in a data processing system for testing hardware in a the data processing system having multiple partitions including a first partition and a second partition, each of the multiple partitions configurable by the data processing system for running an operating system image therein, the method comprising:  
initializing a monitor process in a the first partition assigned to a first processor;  
and  
initializing a random code generation process in a the second partition associated with a second processor, wherein the random code generation process generates instructions and executes the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.
2. (Original) The method of claim 1, wherein the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed.
3. (Original) The method of claim 2, wherein the random code generation process calls a function to store data for the heartbeat in a data structure.
4. (Original) The method of claim 3, wherein the monitor process monitors the random code generation process by checking the data structure.
5. (Original) The method of claim 1, wherein the first processor and the second processor are located in a single chip.
6. (Original) The method of claim 1 further comprising:  
responsive to detecting an error executing the instructions in the second partition,  
preventing termination of the second partition.

7. (Currently amended) A data processing system comprising:  
a bus system;  
a communications unit connected to the bus system;  
a memory system connected to the bus system, wherein the memory system includes a set of instructions comprises a plurality of partitions including a first partition and a second partition, each of the plurality of partitions configurable by the data processing system for running an operating system image therein; and  
a processing unit connected to the bus system, wherein the processing unit executes the set of instructions to initialize a monitor process in a the first partition assigned to a first processor and initialize a random code generation process in a the second partition associated with a second processor in which the random code generation process generates instructions and executes the instructions to test the second processor and in which the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.
8. (Currently amended) A data processing system for testing hardware in a the data processing system has having multiple partitions including a first partition and a second partition, each of the multiple partitions configurable by the data processing system for running an operating system image therein, the data processing system comprising:  
first initializing means for initializing a monitor process in a the first partition assigned to a first processor; and  
second initializing means for initializing a random code generation process in a the second partition associated with a second processor, wherein the random code generation process generates instructions and executes the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.
9. (Original) The data processing system of claim 8, wherein the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed.

10. (Original) The data processing system of claim 9, wherein the random code generation process calls a function to store data for the heartbeat in a data structure.
11. (Original) The data processing system of claim 10, wherein the monitor process monitors the random code generation process by checking the data structure.
12. (Original) The data processing system of claim 8, wherein the first processor and the second processor are located in a single chip.
13. (Original) The data processing system of claim 8 further comprising:  
preventing means, responsive to detecting an error executing the instructions in the second partition, for preventing termination of the second partition.
14. (Currently amended) A computer program product in a computer readable medium for testing hardware in a data processing system having multiple partitions including a first partition and a second partition, each of the multiple partitions configurable by the data processing system for running an operating system image therein, the computer program product comprising:  
first instructions for initializing a monitor process in a the first partition assigned to a first processor; and  
second instructions for initializing a random code generation process in a the second partition associated with a second processor, wherein the random code generation process generates instructions and executes the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.

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